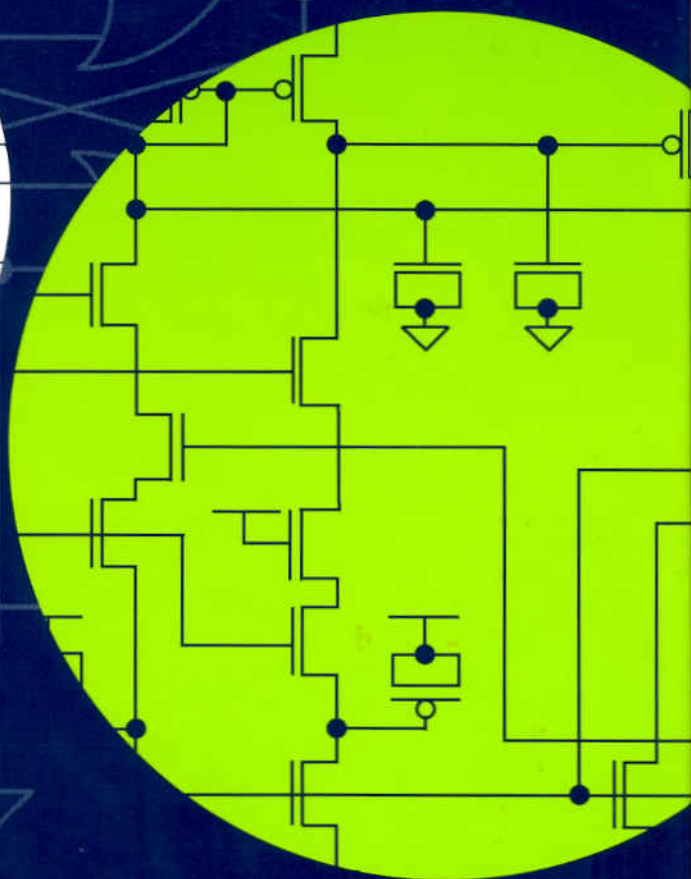
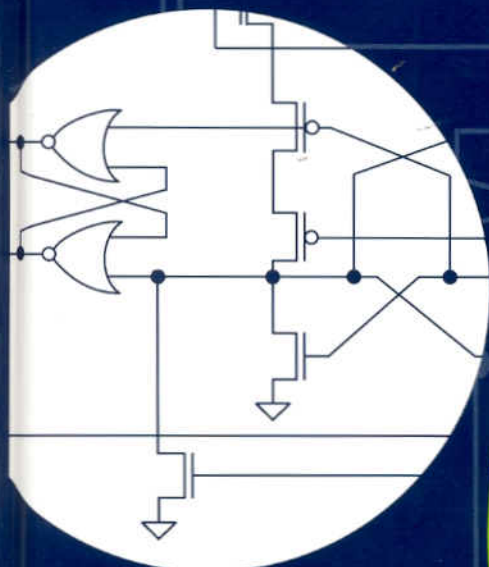


IEEE Press Series on Microelectronic Systems
Stuart K. Tewksbury and Joe E. Brewer, Series Editors

CMOS

CIRCUIT DESIGN, LAYOUT, AND SIMULATION

REVISED SECOND EDITION



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